Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor processing component comprising:

a substrate consisting essentially of (i) SiC or (ii) SiC impregnated with elemental silicon; and

a layer consisting essential of CVD-SiC directly on the substrate, wherein an outer surface portion of the component (i) consists essentially of the CVD-SiC, and (ii) has a surface impurity level that is not greater than 2 times a bulk impurity level, measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The component of claim [[4]]1, wherein the substrate comprises SiC.

6. (Currently Amended) The component of claim [[5]]1, wherein the substrate comprises SiC impregnated with elemental silicon.

7. (Original) The component of claim 6, wherein the substrate comprises recrystallized SiC impregnated with elemental silicon.

8. (Currently Amended) The component of claim [[4]]1, wherein the ~~CVD-SiC~~ layer has a thickness within a range of about 10 to about 1000 μm.

9. (Currently Amended) The component of claim [[4]]1, wherein the ~~CVD-SiC~~ layer has a thickness within a range of about 10 to about 800 μm.

10. (Currently Amended) ~~The component of claim 1,~~ A semiconductor processing component, wherein the component ~~is~~ consists essentially of ~~a free-standing~~ CVD-SiC ~~component~~, wherein an outer surface portion of the component has a surface impurity level that is not greater than 2 times a bulk impurity level, measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Original) The component of claim 1, wherein the surface impurity level is not greater than the bulk impurity level.

15. (Original) The component of claim 1, wherein the surface impurity and bulk impurity levels are based on at least one of Cr, Fe, Cu, Ni Al, Ca, Na, Zn, and Ti concentrations

16. (Original) The component of claim 15, wherein the surface impurity and bulk impurity levels are based on at least one of Cr and Fe concentrations.

17. (Original) The component of claim 16, wherein the surface impurity and bulk impurity levels are based on Fe concentration.

18. (Original) The component of claim 16, wherein the bulk impurity level is not greater than 1E17 atoms/cc Fe and not greater than 1E15 atoms/cc Cr.

19. (Original) The component of claim 1, wherein the semiconductor processing component comprises a component from the group consisting of semiconductor wafer paddles,

process tubes, wafer boats, liners, pedestals, long boats, cantilever rods, wafer carriers, process chambers, dummy wafers, wafer susceptors, focus rings, suspension rings.

20. (~~Previously Presented~~Currently Amended) A wafer boat comprising:

a substrate consisting essentially of SiC impregnated with elemental silicon; and

a layer consisting essential of CVD-SiC directly on the substrate, wherein an outer surface portion of the component (i) consists essentially of CVD-SiC, and (ii) has a surface impurity level that is not greater than 2 times a bulk impurity level, measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

21. (Original) The component of claim 1, wherein the component is machined prior to treatment to provide said surface impurity level.

Claims 22-53 (Canceled)